A Variable Gain and Bandwidth Fully Differential CMOS Neural Preamplifier

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Abstract

The design of a low noise low power fully-differential CMOS preamplifier for bioelectrical signals recording applications is presented. The capacitive-coupled and capacitive-feedback topology is adopted. The amplifier current consumption is 5.2 μA or 18.2 μA at 3 V supply for a mid-band gain of 39.4 dB or 25.9 dB, respectively. Each corner frequency is 2-bit programmable for amplifying biosignals located in different bands. The bandwidth can be extend from 0.15 Hz - 2.68 kHz to 0.03 Hz - 40.4 kHz. To avoid possible saturation at the differential output, a discharged switch is incorporated. The circuit has an input-referred noise of 2.99 μVrms integrated from 0.1 Hz to 10 kHz. It was designed and simulated using 0.5 μm 3M2P CMOS process. The circuit is in the manufacturing process.

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1 Introduction

Over the past three decades it has greatly increased interest in understanding the work and behavior of the human brain by studying its biological signals. By using surface, internal or implantable MEMS multi-channel electrodes, neuroscientists and clinicians have simultaneous records of multiple electrical biosignal activities synchronized. The knowledge obtained from these studies has allowed the detection of possible health problems and new clinical, neuroprosthetic and artificial limb control applications, among others [1, 2].

Due to the high impedance of the recording electrodes up to more than 500 kΩ [3], the electrical interference by outside sources generated by electrical noise elsewhere in the body, poor contact or machine/equipment malfunction

promptly couples to the low level biosignals. To get a clean amplified biopotential signals recordings, the signal to noise ratio of the amplifier should be as high as possible. Therefore, it is mandatory that the input-referred noise of the amplifier be kept below the minimum possible biopotential voltage. Typical biosignal characteristics are described in Table 5 [4]. Furthermore, through to electrochemical effects at the electrode–tissue interface, DC offsets of 0.2–2 V are common across differential recording electrodes [5]. It would be useful to have a robust preamplifier with variable gain as well as tunable wide frequency range that could be used for different types of biopotential signals or different components in one type of signal. A significant amount of integrated biosignal amplifiers have been designed with different constraints such as low noise, low power, low supply voltage and low cut-off frequency [6–17].

However, there is a lack of biosignals amplifier that considers minimizing total harmonic distortion (THD) and at the same time being low noise amplifiers. Based on the integrated single-ended operational transconductance amplifier (OTA) with capacitive couple and capacitive-feedback topology originally proposed by Harrison [6], this paper reports on the design and simulation of a fully integrated low-noise low-power fully-differential preamplifier with adjustable bandwidth and 1-bit gain control, similar to the one proposed by Yin [9], but getting a THD negligible for the full range of potential biopotential amplitudes, shown in Fig. 1. The amplifier has been designed in 0.5μm CMOS, and its functionality has been simulated in detail.

2 Circuit Design

2.1 Fully Differential OTA Design

The low-noise low-power fully differential OTA is shown in Fig. 2a. It has an associated CMFB amplifier [18] (Fig. 2b) to guarantee its outputs common-mode voltage around $V_{CM} = V_{DD}/2$, where V_{DD}=3V. A self-referenced Beta-multiplier is used for biasing wide-swing current mirrors (V_{B1} to V_{B4}) [19]. The power consumption of the current source biasing circuits was not included in the power measurements, since they are also used by another circuits laid out in the same integrated circuit. From analyzing the OTA schematic and assuming that $g_{m1,2} \gg g_{m3,4}$, $g_{m1,2} \gg g_{m5,6}$ and $g_{m1,2} \gg g_{m7,8}$, where g_{mi} is the transconductance of the M_i transistor, the input-referred noise is:

$$\overline{v_{ni,OTA}^2} = \left[\frac{8kT}{3g_{m1}} + \frac{K_{sub}I_{D1}^2}{C'_{ox}W_1L_1g_{m1}^2 f}\right]\Delta f \tag{1}$$

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where k is the Boltzmann's constant, T is the absolute temperature, f is the frequency, K_{sub} is the flicker noise coefficient of a transistor operating in the subthreshold region, C'_{ox} is the gate capacitance per unit area of a transistor, Δf is the integrated bandwidth, I_{Di} is the drain current of M_i, and W_i and L_i are the channel width and length of M_i.

To achieve a low noise amplifier, the input transistors transconductance of the OTA must be maximized while maintaining their current as low as possible. In addition, since the flicker noise in PMOS transistors is lower than in NMOS transistors [20], the amplifier input pair is PMOS.

Each transistor operates in weak, moderate, or strong inversion depending on its ratio and its drain current. Defining the moderate inversion characteristic current I_S and the inversion coefficient IC as [21]:

$$I_S = \frac{2\mu C_{ox} U_T^2}{\kappa} \cdot \frac{W}{L} \tag{2}$$

$$IC = I_D / I_S \tag{3}$$

where U_T is the thermal voltage and κ is the subthreshold gate coupling coefficient, typical value of 0.7. In strong inversion the transistor has a transconductance proportional to the square root of drain current and IC>10. When IC<0.1 the device is in weak inversion and has its transconductance proportional to drain current. For moderate inversion operation 0.1<IC<10 and both strong and weak inversion expressions overestimate transconductance [22]. Based on the EKV model [23], the transconductance can be estimated as:

$$g_m \approx \frac{\kappa I_D}{U_T} \cdot \frac{2}{1 + \sqrt{1 + 4 \cdot IC}} \tag{4}$$

Hence, to minimize the OTA input-referred noise, M_1 and M_2 should operate in weak inversion region, while all other transistors of the OTA operate in strong inversion to meet the assumptions made in the definition of Eq. (1).

2.2 Variable Gain

The mid-band closed-loop differential gain of the amplifier topology used is given by C_1/C_2 (Fig. 1). Since different types of biosignals have a wide amplitude range (Table 5), a 1-bit (B_0) allows to change the gain level. Thus, C_2 is formed by the series combination of C_{2a} and C_{2b}, changing its value from C_2=C_{2a} to C_2= $C_{2a}C_{2b}/(C_{2a} + C_{2b})$ (Fig. 3).

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2.3 High-cutoff Frequency

The dominant low-pass pole occurs at the closed-loop amplifier output nodes. It is given by:

$$f_H = \frac{1}{2\pi R_{out} C_L} = \frac{1}{2\pi (r_{o6} \,||\, r_{o7}) C_L} \tag{5}$$

where C_L is the load capacitance connected at each output node, R_{out} is the OTA output resistance and r_{oi} is the output resistance of the M_i device. Defining $I_{D9} + I_{D11} + I_{D13} = I_{bias}$ and since W_3/L_3=W_4/L_4=W_5/L_5=W_6/L_6 $I_{D6} = I_{D7} = I_{bias}/2$ then $f_H \propto (I_{bias}/2)^{3/2}$.

The OTA operation point can be changed dynamically by 2-bits (B_1-B_2) work on a multiplexer to drive $I_{D11} = I_{D12}$ and $I_{D13} = I_{D14}$ (Fig. 4), whereas $I_{D9} = I_{D10}$ is constant. Thereby, f_H change between four possibles values.

In order to avoid a systematic offset in the common-mode output voltage the current density through $M_7 = M_8$ must be equal to that of M_{20}. Hence the biasing current in the CMFB circuit should be changed in the same proportion that I_{bias} by B_1-B_2 (Fig. 4).

2.4 Low-cutoff Frequency

The dominant high-pass pole is given by:

$$f_L = \frac{1}{2\pi R_{eq} C_2} \tag{6}$$

where R_{eq} is the equivalent resistance given by the series combination of the pseudo-resistors M_P and M_N in Fig. 1.

To achieve a very low-cutoff frequency, very high value of R_{eq} in order of $10^{12}\Omega$ is required. Many previous works use diode-connected MOS [6–8] or subthreshold biased MOS [9–11] to achieve this goal. However they suffer from distortion at high level output

To solve this problem, based on the MOS pseudo-resistor operating in the deep subthreshold region controlled by current described in [24], a digitally controlled current biasing NMOS-PMOS pseudo-resistors M_P and M_N is used. The schematic is shown in Fig. 5, where V_{CM} is a input reference voltage, M_{30} and M_{31} are diode-connected and the output bias voltage V_P and V_N are established by the current through M_{30} and M_{31}, which can be modified with 2-bits (B_3-B_4) using multiplexers similar to those described in Fig. 4.

If the low-noise amplifier (LNA) closed loop gain is modified, it will also change the value of f_L, due to the C_2 variation.

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2.5 Saturation Detector

If there is a considerable noise at the OTA input, it could saturate the CMFB amplifier producing an undesirable V_{CMFB}, which would generate an imbalance in the OTA, causing its outputs to become saturated clamping v_{O+} to ground a v_{O-} to V_{DD}. If this occurs, the recovery time of the OTA and the CMFB amplifier at normal operating conditions would take a long time due to the long settling time associated with the time constant of M_P, M_N and C_2. To overcome this a reset circuit is incorporated using a level shifter followed by an inverter [19] (Fig. 6). When a saturation occurs v_{O+} goes to ground and $V_{SW} = V_{DD}$. Both switches M_{SW} (Fig. 1) are turned on shorting the outputs with the inputs establishing a rapid settling time. In normal operation condition, the output of the level shifter is $(v_{O+} + V_{SG_{35}})$ and $V_{SW} = 0V$.

3 Simulation results

3.1 Amplifier Simulation

In order to fulfill with the established requirements in section 2.1, the size of transistors in the OTA are provided in table 2 and the common-mode voltage is provided externally to V_{CM}=1.5V.

Table 3 summarize the characteristics of the OTA and its CMFB circuit for I_{bias}=2.08 μA and I_{bias}=7.30 μA, which are the minimum and maximum biasing currents in the OTA, as will be described in section 3.3. I_{total} represents the sum of current consumption of the OTA and CMFB.

Since for the software the fully differential OTA is perfectly balanced, the simulated common-mode gain is zero. Then to take into account the offset introduced by the mismatch in the manufacturing process, a systematic offset voltage V_{os}=10 mV was added at one output, obtaining a common-mode rejection ratio (CMRR) of 112 dB and a power-supply rejection ratio (PSRR) of 99 dB both at 1 kHz.

3.2 Closed-loop gain

Setting C_1 to 20 pF, C_{2a} to 1 pF and C_{2b} to 250 fF were chosen to obtain a in-band gain of 39.4 dB for B_0 set to "0" logic and a gain of 25.9 dB for B_0 set to "1" logic.

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3.3 Frequency Response

Through B_1-B_2, the OTA bias current is changed between four possible values between I_{bias}=2.08 μA and I_{bias}=7.30 μA. This change in the operation point condition produces a variation in the high-cutoff frequency from 2.68 kHz to 9.16 kHz for a gain of 39.4 dB and from 12.1 kHz to 40.4 kHz for a gain of 25.9 dB using a load capacitance C_L=15 pF.

B_3-B_4 set the current in the floating current source (Fig. 5). This will change the value of R_{eq} in Eq. (6), adapting the lower cutoff frequency between 0.15Hz and 145Hz with B0="0", and from 0.03Hz to 30Hz with B0="1".

The simulations of the modifiable frequency responses are shown in Fig. 7.

3.4 Noise and distortion

The preamplifier input-referred noise is related to the OTA input-referred noise by

$$\overline{v_{ni,LNA}^2} = 2\left(\frac{C_1 + C_2 + C_{in}}{C_1}\right)^2 \overline{v_{ni,OTA}^2} \tag{7}$$

where C_{in} is the OTA input capacitance. The simulated input-referred noise integrated from 0.1 Hz to 10 kHz was 2.99 μV_{rms} and the total harmonic distortion (THD) stays below 1% for large inputs signal less than 25.2 mV_{pp} for a gain of 25.9 dB. In the case of gain equal to 39.4 dB the simulated input-referred noise was 3.05 μV_{rms} and the 1% THD was produced by signal less that 6.2 mV_{pp}. As shown in Fig. 8 in both cases the thermal noise is 24nV/$\sqrt{Hz}$ and the $1/f$ noise corner frequency occurs at 1 Hz.

3.5 Output Saturation

Fig. 9a shows the simulation for a suddenly increase at the differential input at t = 200 msec. This pulse tend to saturate both OTA outputs, but the output voltage detector turn on M_{SW} and after 50 msec the OTA recover the steady state operation, due to reduction in the time constant associated with M_P, M_N and C_2.

Fig. 9b shows an zoom-in of the saturation event. It is observed that the inverter input follows the value of v_{O+}. When v_{O+} falls below 0.75 V the inverter output change its value turning on M_{SW}.

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4 Discussion

Table 4 shows a comparison between different neural amplifiers. This work presents better input-referred noise and a upper high cut-off frequency than the compared works, allowing to use this amplifier for EEG signals.

Two other important parameters that must be taken into account to get a good biosignal amplifier are the THD and CMRR. This amplifier was designed with great attention to these parameters, achieving better results than the other works.

However, it is observed that the power required by this amplifier is greater than the other amplifiers. This is due to the old CMOS technology used and to achieve better performance.

5 Conclusion

This work present a low-power low-noise fully differential preamplifier for biopotenial recording applications with an input referred noise of 3.05 μV_{rms} (setting the mid-gain to 25.9 dB) and 2.99 μV_{rms} (setting the mid-gain to 39.4 dB) over 0.1 Hz - 10 kHz. It has been designed and simulated based on 0.5μm CMOS technology. The fully integrated amplifier is able to rejects DC offsets voltages frequently found in microelectrode applications. Using 5-bit digital control, the bandpass frequency response (f_L: 0.015 - 0.03 Hz, f_H: 2.68 - 40.4 kHz) and variable gain (19.9 dB and 39.4 dB) are adjusted to offer the amplifier's capabilities to amplify different biomedical signals. The layout was sent for fabrication. Future work includes making measurements on the manufactured circuit and changing this designed circuit to a technology below 180 nm in order to reduce power consumption and get better NEF.

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Biopotential	**Frequency Range**	**Amplitude Range**
Electrocardiogram (ECG)	0.05 - 100 Hz	1 - 5 mV
Electroencephalography (EEG)	0.5 - 40 Hz	0.5 - 100 μV
Electromyography (EMG)	20 Hz - 2 kHz	1 - 10 mV
Extracellular neural action potentials (ENAP)	0.1 Hz - 10 kHz	50 - 500 μV
Electrooculography (EOG)	DC - 10 Hz	10 - 100 μV

Table 1: Biosignals characteristics

Device	**W/L** [μ**m**]
M_1, M_2	300/1.5
M_3, M_4, M_5, M_6	9/15
M_7, M_8	18/15
M_9, M_{10}, M_{33}	72/30
M_{11}, M_{12}	72/60
M_{13}, M_{14}	144/60
M_{15}, M_{16}, M_{17}, M_{18}	36/15
M_{19}, M_{20}	9/15
M_{21}, M_{22}, M_{28}	18/30
M_{23}, M_{24}, M_{25}, M_{26}	18/60
M_{27}, M_{SW}	9/30
M_{29}, M_{32}	36/30
M_{30}, M_{31}	750/1.5
M_{34}	144/30
M_{35}	36/3
M_{36}	36/90
M_{37}	9/9
M_{38}	90/9
M_{C2}	3/0.6
M_P, M_N	4.5/180

Table 2: Transistor size

I_{bias}	2.08 μA	7.30 μA
OTA open loop gain	60.3 dB	62.4 dB
OTA phase margin	82.7^{o}	76.0^{o}
OTA GBW	278 kHz	897 kHz
CMFB GBW	65 kHz	431 kHz
input-referred noise (0.1 Hz - 10kHz)	$4.79\mu V_{rms}$	$2.22\mu V_{rms}$
I_{total}	5.2 μA	18.2 μA

Table 3: OTA characteristics for both boundary operation conditions

	This work	Maghami [17]	Kim [16]	Valtierra [15]	Gagnon [13]	Yang [14]
Power supply [V]	3	1.8	1	1	1.2	1
Max current consumption [μA]	5.2 - 18.2	20.4	2.28	0.815	2.33	2.85
Max power consumption [μW]	54.6	36.7	2.28	0.815	2.8	2.85
Gain [dB]	25.9 - 39.4	79.8 - 87	43 - 61	40.4	46	58.7
Low frequency cutoff [Hz]	0.03 - 0.15	11 - 90	1 - 220	1 - 200	0.5 - 400	0.49
High frequency cutoff [kHz]	2.68 - 40.4	6.2 - 10	0.53 - 8.9	0.7 - 5	7	10.5
CMRR [dB]	112	-	90.2	58 - 68	71.7	>45
PMRR [dB]	99	-	77.8	-	-	>50
Input-referred noise [μV_{rms}]	2.99 (0.1 Hz -10 kHz)	4 (1 Hz - 10 kHz)	4.74 (1 Hz - 10 kHz)	4.1 (200 Hz - 5 kHz)	3.2 (10 Hz -10 kHz)	3.04 (0.1 Hz -100 kHz)
THD (%)	1% (6.2 - 25.2 mVpp input)	0.32% (95 μVpp input)	-	<1% (1mVpp input)	0.95% (5 mVpp input)	1.6% (1 mVpp input)
Noise efficiency factor (NEF)	4.89	6.8	2.91	2.02	2.30	3.86 *
CMOS technology	0.5 μm	0.18 μm	0.18 μm	0.18 μm	0.13 μm	90 nm

* [14] report a NEF=1.93 calculated over a $100kHz$ bandwidth, different from the amplifier bandwidth.

Table 4: Comparison with other analog front-end for biosignals applications

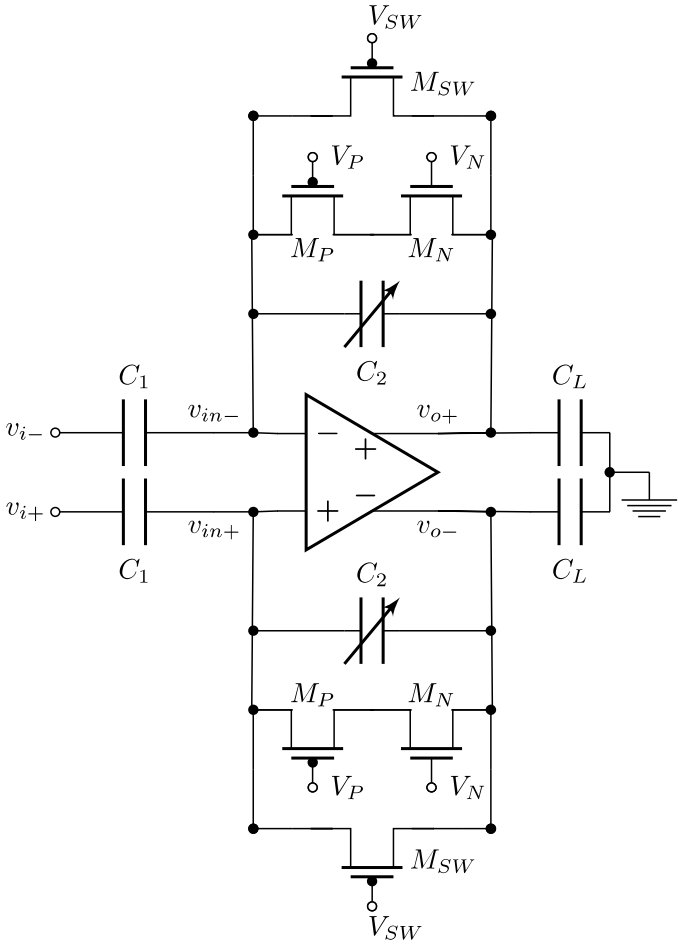
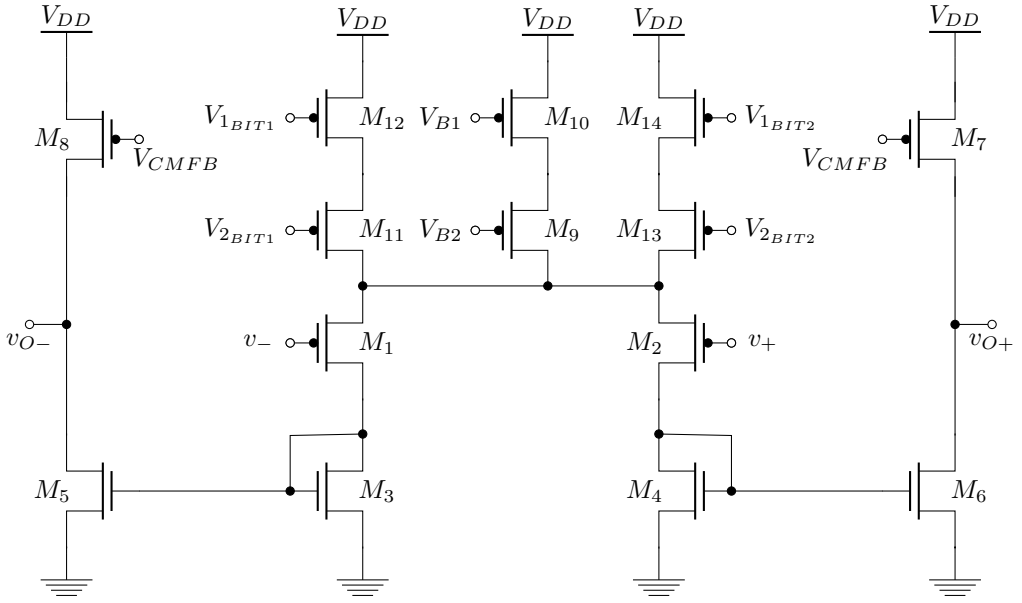
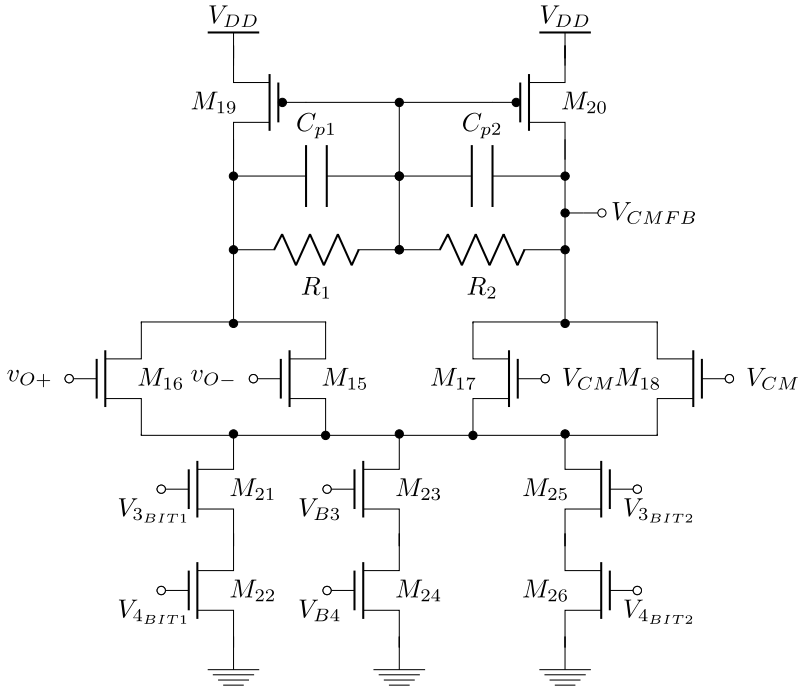


Figure 1: Proposed fully-differential biosignal amplifier



(a)



(b)

Figure 2: Schematic of the (a) fully-differential OTA with (b) its CMFB circuit

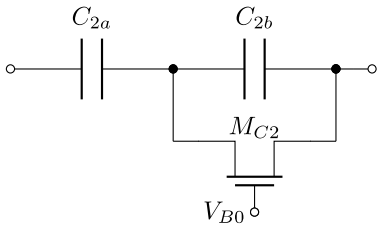


Figure 3: Equivalent variable capacitors to C_2

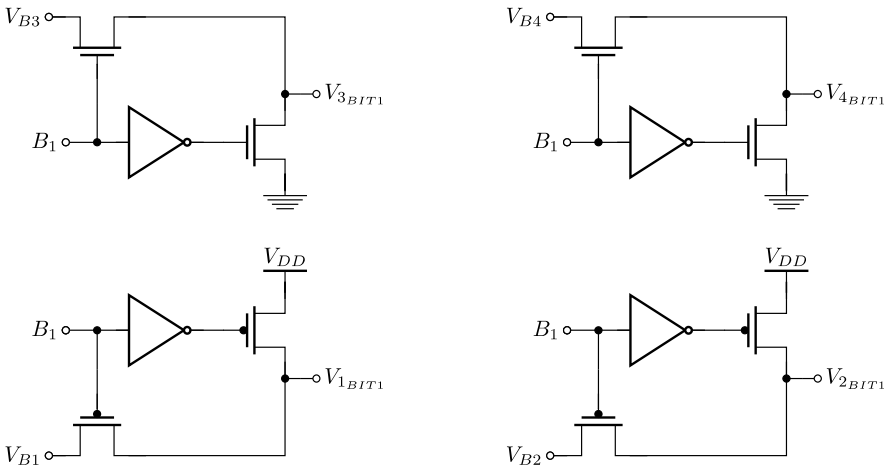


Figure 4: B1 multiplexer to switch on / off current sources

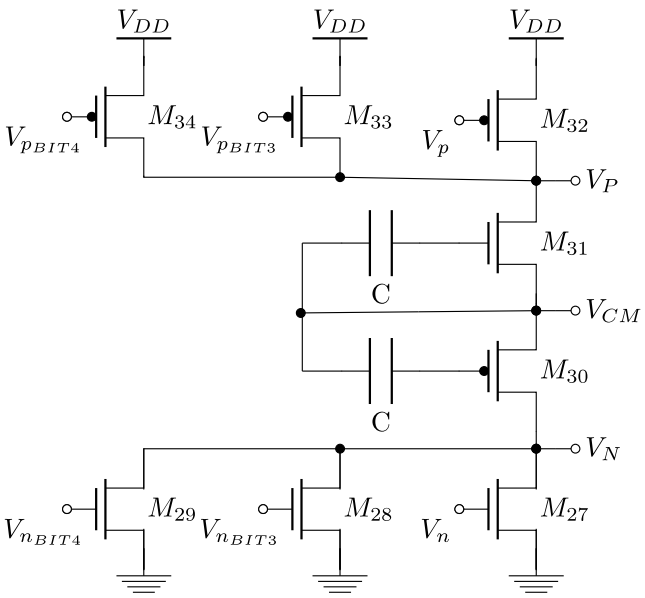


Figure 5: Floating current source to generate V_P and V_N

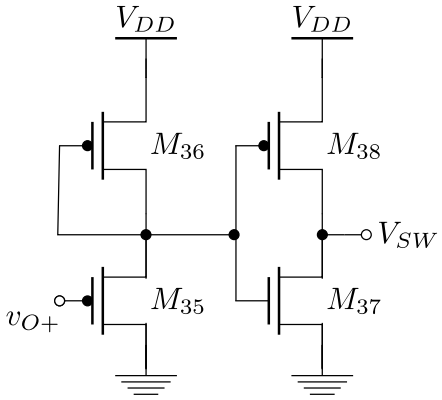
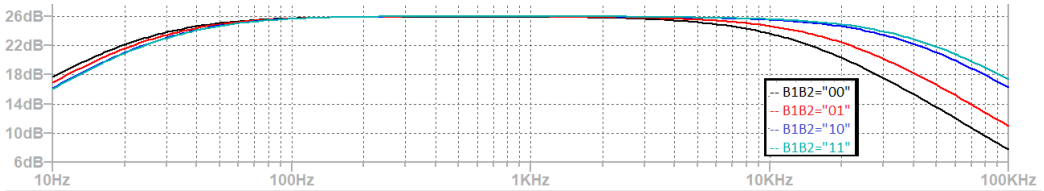
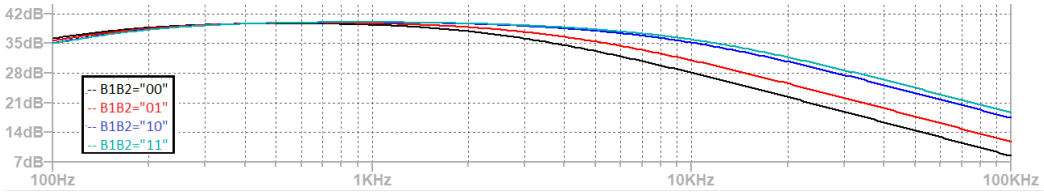


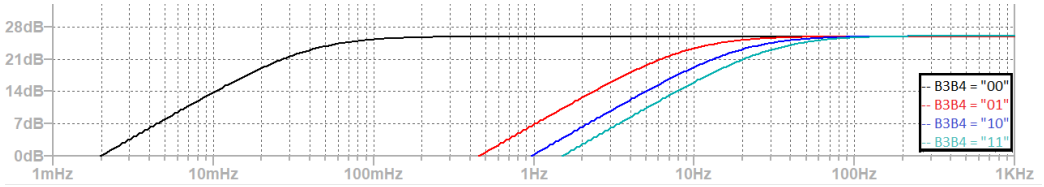
Figure 6: Output voltage detector circuit



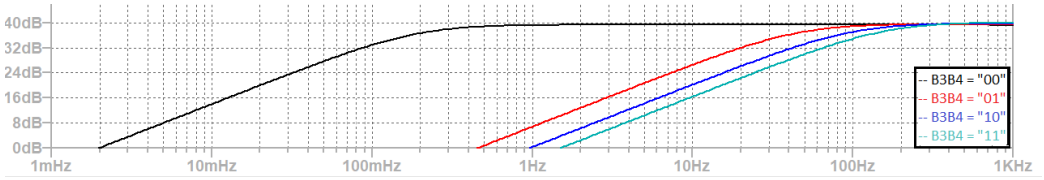
(a)



(b)



(c)



(d)

Figure 7: High-cutoff band-pass frequency response of the LNA for a (a): Gain=25.9 dB and for a (b): Gain=39.4 dB. Low-cutoff band-pass frequency response of the LNA for a (c): Gain=25.9 dB and for a (d): Gain=39.4 dB

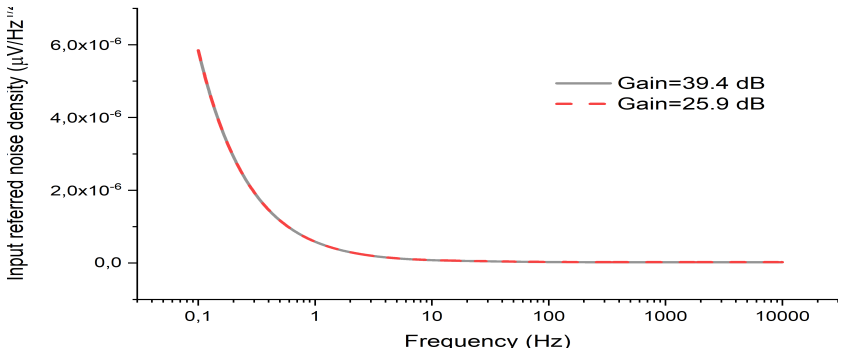
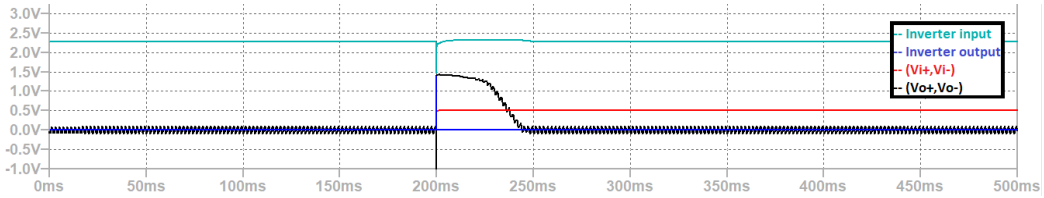
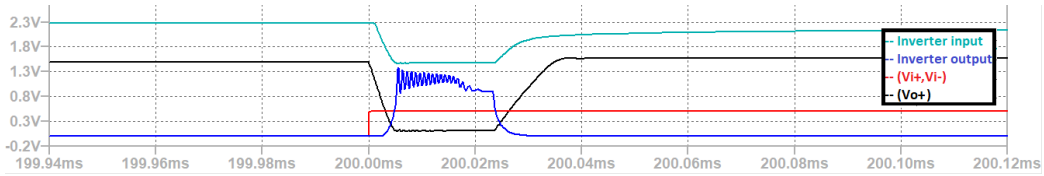


Figure 8: Simulated LNA input-referred voltage noise for maximum bandwidth settings



(a)



(b)

Figure 9: Recovery response to an output saturation